CLAIMS:

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. In a computer system having a processor with a plurality of activity states, and at least one peripheral device in operative relation with the processor, a method of operating the computer system comprising communicating the activity state of the processor to the at least one peripheral device.

2. A method as recited in claim 1, further comprising:
supplying an interrupt from the peripheral to the processor when the processor changes activity states from a first activity state to a second activity state.

3. A method as recited in claim 2, further comprising detection of the activity state of the processor by the peripheral before said interrupt is supplied.

4. A method as recited in claim 2, wherein said supplying of said interrupt is performed only if said peripheral needs to be serviced by said processor.

5. A method as recited in claim 2, wherein the peripheral has a plurality of urgency states and an activity state of the processor is evaluated against

the urgency state of the peripheral to determine whether said peripheral issues an interrupt.

6. A method as recited in claim 5, wherein if said urgency state of said peripheral is high, said peripheral issues an interrupt to said processor regardless of said activity state of said processor.

7. A method as recited in claim 5, wherein if said urgency state of said peripheral is low, said peripheral issues an interrupt to said processor only if said activity state of said processor is other than low.

8. A method as recited in claim 2, wherein a plurality of peripherals are in operative relation with said processor, and a peripheral has issued an interrupt request to said processor, the method further comprises:

issuing interrupt requests to said processor from all peripherals which need to be serviced; and

servicing all of said interrupt requests by said processor.

9. A method as recited in claim 8, wherein said interrupt requests are serviced by the processor before the processor changes its activity state.

10. A method as recited in claim 8, further comprising setting the urgency level of each of the peripherals

that have been serviced to a lowest urgency level after the peripheral has been serviced.

11. A method as recited in claim 1, wherein the activity states of the processor are represented by at least one bit output of the processor.

12. A method as recited in claim 1, wherein the activity states of the processor are represented by at least one output word generated by the processor.

13. A method as recited in claim 1, wherein the activity state of the processor is communicated as being in a state selected from active, idle and sleep.

14. A computer system having a processor with a plurality of activity states, in which interrupts from at least one peripheral in operative relation with the processor are serviced, the system comprising means for communicating the activity state of the processor to the at least one peripheral.

15. A system as recited in claim 14, further comprising means for supplying an interrupt from the peripheral to the processor when the processor changes activity states from a first activity state to a second activity state.

16. A system as recited in claim 15, further comprising detection means associated with the peripheral for detecting the activity state of the processor before said interrupt is supplied.

17. A system as recited in claim 15, wherein said means for supplying said interrupt supplies said interrupt only if said peripheral needs to be serviced by said processor.

18. A system as recited in claim 15, wherein the peripheral has a plurality of urgency states, further comprising means for evaluating an activity state of the processor against the urgency state of the peripheral to determine whether said peripheral issues an interrupt.

19. A system as recited in claim 18, wherein if said urgency state of said peripheral is high, said peripheral issues an interrupt to said processor regardless of said activity state of said processor.

20. A system as recited in claim 18, wherein if said urgency state of said peripheral is low, said peripheral issues an interrupt to said processor only if said activity state of said processor is other than low.

21. A system as recited in claim 14, further comprising:

a plurality of peripherals in operative relation with said processor;

means for said processor to receive interrupt requests from all of said additional peripherals, when said peripherals need to be serviced; and

means operatively connected with the processor for servicing all of said interrupt requests.

22. A system as recited in claim 21, wherein said means for servicing said interrupt requests services said interrupt requests before the processor changes its activity state.

23. A system as recited in claim 21, further comprising:

means for setting the urgency level of each of the peripherals that have been serviced to a lowest urgency level after the peripheral has been serviced.

24. A system as recited in claim 14, wherein the activity states of the processor are represented by at least one bit output of the processor.

25. A system as recited in claim 14, wherein the activity states of the processor are represented by at least one output word generated by the processor.

26. A system as recited in claim 14, wherein the processor has activity states selected from active, idle and sleep.

27. A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing the computer to effect a method for operating the computer system to service interrupts from a peripheral in operative relation with a processor having a plurality of activity states, the method comprising communicating the activity state of the processor to the at least one peripheral.

28. A computer program product as recited in claim 27, further comprising computer readable program code means embodied therein for causing the computer to supply an interrupt from the peripheral to the processor, when the processor changes activity states from a first activity state to a second activity state.

29. A computer program product as recited in claim 21, further comprising computer readable program code means embodied therein for detecting the activity state of the processor.

30. A computer program product as recited in claim 28, further comprising computer readable program code for supplying of said interrupt only if said peripheral needs to be serviced by said processor.

31. A computer program product as recited in claim 28, wherein the peripheral has a plurality of urgency

states, further comprising computer readable program code for evaluating an activity state of the processor against the urgency state of the peripheral, to determine whether said peripheral issues an interrupt.

32. A computer program product as recited in claim 31, further comprising computer readable program code which if said urgency state of said peripheral is high, causes said peripheral to issue an interrupt to said processor regardless of said activity state of said processor.

33. A computer program product as recited in claim 31, wherein if said urgency state of said peripheral is low, said peripheral issues an interrupt to said processor only if said activity state of said processor is other than low.

34. A computer program product as recited in claim 27, wherein a plurality of peripherals are in operative relation with said processor, and a peripheral has issued an interrupt request to said processor, the computer readable program code further comprises code for:

issuing interrupt requests to said processor from all peripherals which need to be serviced; and

servicing all of said interrupt requests by said processor.

35. A computer program product as recited in claim 34, comprising computer readable program code for servicing said interrupt requests computer readable program code before the processor changes its activity state.

36. A computer program product as recited in claim 34, further comprising computer readable program code for setting the urgency level of each of the peripherals that have been serviced to a lowest urgency level after the peripheral has been serviced.

37. A computer program product as recited in claim 27, comprising computer readable program code wherein the activity states of the processor are represented by at least one bit output of the processor.

38. A computer program product as recited in claim 27, further comprising computer readable program code wherein the activity states of the processor are represented by at least one output word generated by the processor.

39. A computer program product as recited in claim 27, comprising computer readable program code for detecting the processor state as a state selected from active, idle and sleep.